Vivado ML Enterprise

Device Support

- Versal™ AI Core Series: - XCVC1902 and XCVC1802
- Versal Prime Series: - XCVM1802
- Virtex® UltraScale+™ HBM device: XCVU57P

Install and Licensing

- **Flexlm version upgraded to 11.17.2.0**
  - Support 64-bit versions of Linux and Windows only
  - Customer using floating license must upgrade licensing utilities to Flexlm 11.17.2.0

IP Integrator

- **Block Design Container**
  - 2021.1 is the production release for block design containers.
  - Enables Modular Designing for Reusability
  - Allows Team Based Designs
  - Enables DFX Flow in the Project Mode
  - Ability to specify variants for simulation and synthesis
  - Address management for BDCs from the Top-level BD

- **Vivado Store**
  - Download boards and example designs from GitHub
  - 3rd party board partners can contribute to these repositories asynchronously to Vivado releases
- **IP/IPI Revision Control Improvements**
  - Migration of older Vivado projects to new directory structure
- **CIPS 3.0**
  - IP Re-architecture of CIPS to Hierarchical Model
  - New Modular User Interface

Vivado Text Editor – Sigasi Backend

- Language protocol server supporting:
  - Autocomplete
  - Go to Definition / Find Usages
  - Tool-tips
  - Indent (Range only in VHDL)
  - Syntax Errors and Warnings as you type
  - Code folding
  - Semantic Highlighting

- **IPI Designer Assistance for CIPS & NoC**
  - Enables intuitive Block Automation for NoC & CIPS connectivity
  - Allows easier creation of designs that access all available memory connected to the device or on the board, e.g. DDR and LPDDR
- **Non-Power of 2 DDR Assignment through Interconnect**
  - IPI now supports non-power-of-2 (NPOT) address assignments across Address Paths with one or more SmartConnect IP

IP Enhancements

- **IP Packager Enhancements**
  - Packager customer experience improvements
    - Connectivity of custom interfaces in IPI / Custom IP
    - XPM memory in the packager
    - Ability to tag files as SV or VHDL-2008 in the packager from package an IP from a directory
  - Production release for packaged RTL IP as Vitis kernel
    - Kernel specific DRCs within IP packager
    - Ease of use
    - Preservation of metadata in these packaged IPs for Vitis kernel usage

- **IP Enhancements – Data Center**
  - PCIe Subsystems
    - Early access support for CPM5, PL PCIE5, and GTYP in Versal Premium
    - CPM4 support in Versal CIPS Verification IP (VIP) for simulation
  - Introducing the Algorithmic CAM IP
    - EA for US+ devices
  - AXI IIC improvement to dynamic read mode function
  - SmartConnect support for non-power-of-two address ranges
  - XilSEM library API release & documentation in UG643
  - SEM IP core device support additions for US+ devices

- **IP Enhancements – Video and Imaging**
  - Video and Image Interface IPs
    - CSI TX subsystem adds support for YUV422 10bit
    - DisplayPort Subsystems add support for HDCP2.2/2.3 repeater feature
    - HDMI2.1 (controlled access) adds support for Dynamic HDR, and enhanced gaming features (VRR, FVA, QMS and ALLM)
  - New IP: Warp Processor for digitally manipulating images
    - Supports Keystone distortion, Barrel and Pincushion distortions and Arbitrary distortions
    - Scaling: 0.5x, 1x, 2x; Rotation: -90 to +90 deg
    - Resolutions from 320x240 to 3840x2160, with multichannel support
    - Input and Output: 8/10/12 bpc YUV, RGB

- **IP Enhancements - Wired**
  - 100G Multirate Ethernet Subsystem - MRMAC
    - 10G/25G/40G/50G/100G Ethernet NRZ GTM
    - MRMAC 25G Ethernet at –1LP

- **IP Enhancements – Wireless**
  - O-RAN
    - Static/Dynamic Compression/Decompression Function in the IP core (BFP + Modulation)
    - New interface to support LTE Section Extension Type 3 information and feed an external LTE precoding block through a single interface
    - Support for Beam ID mapping per Slot (in addition to existing per Symbol method)
    - Support for DL Section Type 3 messages
    - Section Type 0 added to PDxCH BID port
    - Max Ethernet packet size increased to 16000 bytes (Support for 9600 byte jumbo frames)

- **IP Enhancements – Storage**
  - NVMeHA now supports Versal and VU23P devices
  - NVMeTC now supports Versal and VU23P devices
  - ERNIC now supports Versal
    - Native connection to the MRMAC
  - AES-XTS available only by special request

- **IP Enhancements XPM**
  - XPM_Memory and EMG now support all URAM sizes
  - XPM_Memory and EMG now support mixed RAM combinations
    - Use ram_style = "mixed"
  - XPM_Memory and XPM_FIFO allow disabling of assertions for broader simulation support
    - DISABLE_XPM_ASSERTIONS define has been added

- **IP Enhancements - GT Wizard**
  - Versal GTY Wizard Production
  - Versal GTYP Wizard available as EA
  - Versal GTM Wizard available as EA

Vitis HLS

- Vitis HLS 2021.1 – Production Versal Support
- Versal timing calibration and new controls for DSP block native floating-point operations
- Flushable pipeline option with lower fanout logic (free running pipeline a.k.a. frp)
- Enhanced automatic memory partitioning algorithm and new config_array_partition option
- New “Flow Navigator” in GUI and merged views for synthesis, analysis and debug
- Vitis flow “never ending” streaming kernel support for low runtime overhead
- Function call graph viewer with heatmap for II, latency and DSP/BRAM utilization
- New synthesis report section for BIND_OP and BIND_STORAGE
- Improved data-driven pragma handling for better consistency
- Vivado report and new export IP widgets to pass options to Vivado
- New text report after C synthesis to reflect GUI information

Logic Synthesis

ML model Integration

- Machine Learning models to predict and select optimizations
  - 30% compilation speedup for Versal designs

New Synthesis Features

- XPM_MEMORY supports heterogeneous RAM mapping
  - Memory array mapped using all device resource types: UltraRAM, Block RAM, and LUTRAM
  - Most efficient use of all resources
  - Use parameter or generic: MEMORY_PRIMITIVE("mixed")
  - Does not support WRITE_MODE = NO_CHANGE
  - VHDL-2008: new support for the to_string() function
  - Log report includes RTL overrides of IP generics and parameters

Implementation

Machine Learning models in implementation

- Predict routing congestion and route delays
- Better correlation between placement-based estimation and actual routing à better Fmax and reduced compile times

opt_design -resynth_remap

- New timing-driven logic cone resynthesis optimizations that reduce logic levels

Manually retime LUTs and registers during placement with XDC properties

- PSIP_RETIMING_BACKWARD
- PSIP_RETIMING_FORWARD

New Features for Versal Devices

- Calibrated Deskew adjusts the clock network delay taps before device startup to further minimize skew
- Automatic pipeline insertion improves clock speed by on paths…
  - Between PL and NoC and between PL and AI Engines
  - Available both from the AXI Regslice IP and by using auto-pipeline properties
  - Adds latency to pipelined paths
- Elastic pipelines from shift register primitives (SRLs)
  - pipelines are built around an SRL which holds excess pipeline stages
  - Placer builds the ideal pipeline based on source and destination placement
  - Stages can be pulled out of the SRL to cover a wider distance
  - Stages are absorbed by the SRL to shrink the pipeline for shorter distances
  - Preserves latency on pipelined paths

Intelligent Design Runs:

- Intelligent Design Runs (IDR) gives pushbutton access to a new, powerful automated timing closure flow
  - report_qor_suggestions
  - ML strategy prediction
  - Incremental Compile
- Available in Vivado projects and is launched by a right-click menu selection of an implementation run that fails timing. The IDR Reports dashboard details the flow progress and provides hyperlinks to the related reports.A great option for users with timing closure difficulty
  - QoR gain average >10%

Report QoR Suggestions (RQS) Improvements

- DFX-aware QoR suggestions
  - Suggestions given only on DFX modules when static is locked
  - No suggestions that disrupt DFX boundaries
  - Synthesis suggestions correctly scoped to global or out-of-context runs
- Assessment included in the interactive report_qor_suggestions (RQS) GUI report

Methodology Violations in Timing Reports

- Timing reports now include Report Methodology summary
  - Draws attention to methodology violations
  - Neglected methodology violations may cause timing failures
- Includes the summary of the methodology violations from the latest report_methodology run
  - Methodology violations summary stored with design checkpoint

New Constraint Reporting Features

- report_constant_path: new command to identify the source of constant logic values observed on cells and pins
  - report_constant_path <pins_or_cells_objects>
  - report_constant_path -of_objects [get_constant_path <pins_or_cells_objects>]

Dynamic Function eXchange

DFX for Versal

- Versal DFX flows available with production status
  - Compile DFX designs from block designs to device image creation
  - Use Vivado IPI Block Design Containers (BDC) for creating Versal DFX designs
- Leverage DFX IP in Versal just as with UltraScale, UltraScale+
  - DFX Decoupler IP, DFX AXI Shutdown Manager IP to isolate non-NoC interfaces
- All programmable logic is partially reconfigurable
  - From NoC to clocks to hard blocks
- AIE full array Dynamic Function eXchange support
  - Supported through Vitis platform flows

BDC for DFX

- Block Design Containers (BDC) for DFX released in IP Integrator
  - Supports all architectures, critical for Versal
- Place a block design within a block design to create and process DFX designs
  - UG947 shows IPI BDC tutorials for Zynq UltraScale+ and Versal devices
  - More DFX tutorials to be posted on GitHub

Classic SoC Boot Flow Using DFX

- Classic SoC Boot flow available for Versal designs
  - Enables users to quickly boot their DDR-based processing subsystem and memory to run Linux prior to loading the programmable logic
  - Separate programming events in Versal to emulate the Zynq boot flow
  - Auto-Pblock generation used in this flow
  - Not compatible with CPM

Versal Tandem configuration for CPM4

- Tandem PROM and Tandem PCIe for CPM4 available
- Users who require 120ms configuration of a PCIe end point now have a selection in the CIPS customization GUI to select the Tandem Configuration mode
    - Tandem PROM – load both stages from flash
    - Tandem PCIe – load stage 1 from flash, stage 2 over PCIe link via DMA
    - None – standard boot

Abstract Shell Support for Nested DFX Designs in UltraScale+

- Subdivide your Reconfigurable Partition (RP) into multiple nested RPs using Nested DFX (pr_subdivide)
- Create Abstract Shell for each nested RP (write_abstract_shell)
- Accelerate the implementation of each Nested RP by using its Abstract Shell

Simulation

- **VHDL-2008 Enhancements**
    - Unconstrained Arrays
    - Conditional Operators
    - Unary Reduction Operators
- **Code Coverage Support**
    - write_xsim_coverage command support for writing intermediate coverage database

Hardware Debug

SmartLynq+ module

- Optimized for Versal High-Speed Debug Port (HSDP)
    - Faster device programming & Memory access
    - High speed data upload & download
    - Data storage: 14GB DDR memory on module
- High-Speed Debug Port (HSDP) Support
    - Support for connecting to Aurora based HSDP over USB-C connector
- PC4 and USB based JTAG
- Serial UART support

ChipScope

- Open-Source Python API for ChipScope
    - Control and communicate with Versal Device and Debug Cores
    - Vivado not required to use – just need a PDI/LTX
    - Benefits
        - Build custom debug interfaces
        - Interface with python ecosystem